APPLICATION

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TITLE: POWER SAVING

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POWER SAVING

TECHNICAL FIELD

This invention relates to power saving.

BACKGROUND

The Universal Serial Bus (USB) is designed to support asynchronous connection and disconnection between electronic and a USB host. The host is typically a computer. Connection or disconnection may be sensed by a computer or central processing unit (CPU) by monitoring the five volts present on the incoming USB cable shielding.

One method for monitoring the connect state of a USB connection (such as the Intel® SA110 palm device microprocessor) is to connect the USB cable to a general purpose input/output (GPIO) that has a weak pull-down. When the cable state changes (connect to disconnect or vice versa) the GPIO changes state (from low to high on a connect, and vice versa for a disconnect.) This state change can generate an interrupt to a controller and appropriate steps taken. In the case of a disconnect, the interrupt results in the USB input being disabled so as to prevent power burn due to floating inputs.

Many low-power devices connectable to a host have a SLEEP mode whereby power to a CPU or controller in the device is shut off to conserve power while the I/O circuit remains powered up. Under these conditions, the inputs to the USB and some GPIO ports are typically not powered down so that they may remain able to detect a WAKEUP signal or for other purposes. During SLEEP, these inputs can float from state to state while awaiting a WAKEUP signal from a host, thus resulting in power burn. Additionally, the USB cable may be removed or come off during SLEEP, which condition the device should be able to recognize.

A pull-down or a pull-up is provided on the inputs of some devices to prevent float, but to wake the device up through the D+ USB input the external host must pull the D+ line low/high for 100 ms resulting in power consumption in the device while the pull-up/pull-down is being overcome by the external host. For a host fighting an internal square device on an integrated circuit (such as a transistor), the current drain can range from 150uA to 1mA.

DESCRIPTION OF DRAWINGS

FIG. 1 is a circuit diagram of an exemplary embodiment.

DETAILED DESCRIPTION

Referring to FIG. 1 an exemplary embodiment of a USB cable disconnect and WAKEUP mode power save circuit 10 is shown as implemented in a microchip.

The circuit 10 has two main sections: a keeper stage 11 and an output buffer stage 13. The circuit 10 is supplied with power from a supply source 15 and ground 17. The circuit has signals ENABLE 12, DATA 14, SLEEP 16, PAD 18, PADIN 20 and USB Host 22. (PAD refers simply to signal line on an integrated circuit chip that is connected to the integrated circuit package via a thin bond wire. In this case, the PAD is connectable to an external USB Host.) The output buffer stage includes buffer control circuit 24 which controls output buffer drivers 26 and 28. Weak pull-up device 30 serves as a controllable weak pull-up, while weak pull-down device 32 serves as a controllable weak pull-down. In an integrated circuit, these may be implemented as square devices (transistors). By "weak" it is meant that the keeper stage 11 supplies only a limited current to hold a particular logic state, which current can be overcome by the USB Host 22 top drive the keeper stage 11 to a different logical state. Typically, this current is in the range of 100uA to 1.5 mA.

While SLEEP 16 is high, the keeper stage 11 weakly holds the last in time state of PAD 18. Weak means that the keeper stage 11 supplies only a limited current to hold a particular logic state, which current can be overcome by the USB Host 22. Typically, this current is in the range of 100uA to 1.5 mA. While SLEEP 16 is low, the holding function of keeper stage 11 is disabled.

NAND gate 34 has as one input SLEEP signal 16, and NOR gate 36 has as one input the inverted SLEEP 16, inverted by inverting buffer 38.

Whenever SLEEP 16 is low, the output of NAND gate 34 is high, turning off controllable weak pull-up device 30, and the output of NOR gate 34 is driven low by the inverted SLEEP 16, turning off weak controllable pull-down 32. This effectively disables the holding function of the keeper stage whenever SLEEP 16 is low.

While SLEEP is high, the output of NAND gate 34 depends upon the state of PAD 18: if PAD 18 is high, then the output 46 of NAND gate 34 is low, turning on controllable weak pull-up device 30 (at the same time controllable weak pull-down 32 is turned off) latching and holding PAD 18 high. If PAD 18 is low, then the output 46 of NAND gate 34 is high, turning off controllable weak

pull-up device 30 (while at the same time controllable weak pull-down 32 is turned on).

Similarly, while SLEEP 16 is high, inverted SLEEP 16 from inverting buffer 42 is lo, thus causing the output 48 of NOR gate 36 to depend on the state of PAD 18. If PAD 18 is high, then the output 48 of NOR gate 36 is low, shutting off controllable weak pull-down 32. When PAD 18 is driven low (for example, by USB Host 22) the output 48 of NOR gate 36 is high, thus turning on controllable weak pull-down 32.

While SLEEP 16 is high, whatever the weakly held state of PAD 18 may be, if PAD 18 is either driven to a different state by USB host 22 or driven during ENABLE high during a time when the local device is controlling the data line, after a brief interval the keeper stage 11 changes to and holds the new (most recent) state of USB host 22 in PAD 18. USB host 22 should be capable of supplying sufficient current to be able to overcome the weakly held state of PAD 18.

When controllable weak pull-up device 30 is on, controllable weak pull-down device 32 device 32 is off, and vice versa. They are both off when SLEEP 16 low, thus disabling the KEEPER 11 stage.

When ENABLE 12 is high and SLEEP 16 is low, PAD 18 is controlled by the output buffer 13 which includes output

buffer drivers 26 and 28. When ENABLE 12 and SLEEP 16 are both low (listen mode), PAD 18 may be driven by USB Host 22 and the output buffers 26 and 28 are shut off. Regardless of the state of ENABLE 12, while SLEEP 16 is high, PAD 18 is held weakly at its last in time state. If, while SLEEP 16 high, the USB host 22 drives PAD 18 high (overcoming the weak pull-down if the saved state was low) the local device CPU (not shown) may be awakened.

Using a circuit of this type saves the need to use valuable GPIO circuitry simply for cable detects. Cable detects may be performed by a software timeout condition.

Table 1 shows a logic state chart for the circuit. References to chip refer to the local device CPU (not shown).

<u>Table 1</u>

EN	D	Sleep	PAD	PADIN	USB Host	Comment
0	X	0	Z	*	Z	Chip listening to USB host and USB host not driving anything
0	X	0	1	0	1	Chip listening to USB host and USB host driving 1
0	X	0	0	1	0	Chip listening to USB host and USB host driving 0
1	0	0	0	1	0	Chip signaling to USB host via D=0 and also reading back via PADIN
1	1	0	1	0	1	Chip signaling to USB host via D=1 and also reading back via PADIN
X	X	1	WX	X	Z	Chip in sleep mode waiting to be woken up via USB host. Host sleeping
X	X	1	1	0	1	Chip in sleep mode waiting to be woken up via USB host. Host waking up
X	X	1	1	1	0	Chip in sleep mode waiting to be woken up via USB host. Host waiting

Legend:
D= Data
EN=Enable
Z => tristated
* => indeterminate
X => either high or low
W => weak signal strength.

WX means weakly driven high or low. While SLEEP 16 is high, when PAD 18 = WX it is weakly holding whatever was sent out/in most recently, but this can be overridden by the USB host 22. For example if the USB host 22 drives a 1 when EN=0 and then goes to Z after that, PAD 18 will remain at W1. If the USB host 22 is at Z and EN=1 and the chip drives a 0 through DATA 14 out to PAD 18, that 0 will remain in PAD 18 as W0 after EN=0.

While SLEEP is high, The state of PAD 18 is weakly held and prevented from floating whenever it is not being driven by PAD.

Other embodiments are within the scope of the claims. For example, the circuit could be implemented with discrete electronic devices rather than in a microchip. The controllable weak pull-up device and the controllable weak pull-down device could include a resistive element.